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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,995	08/29/2003	Thomas R. Bednar	BUR920020107US1	1994

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,995	BEDNAR ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1020* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-15 and 17-20* is/are rejected.

7)☒ Claim(s) *9 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/604,995 filed 08/29/2003.

2. Claims 1-20 remain pending in the Application.

3. Applicant's arguments, see amendment, filed 01/03/2006, with respect to the rejection(s) of claim(s) 1-8, 10-15 and 17-20 under 35 USC § 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

Claim Objections

4. Claims 2-9, 11-17, 19 and 20 are objected to because of the following informalities: mentioned claims have insufficient antecedent basis issue. Each of this claims starts with indefinite article "An" or "A", which should be replaced by –The--

Claims 2 and 19 are objected to because of the following informalities: it is not clear what the Applicant intend to mean by "each of at least some of said plurality of wires . . ."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 10 and 18 rejected under 35 U.S.C. 102(b) as being anticipated by Jacobs et al. (US Patent 4,811,082).

With respect to claims 1, 10 Jacobs et al. teaches an integrated circuit having a plurality of circuits that include at least one I/O circuit and at least one logic circuit (col. 4, ll.22-27), comprising: a) a contact layer having a plurality of contacts for electrically connecting the integrated circuit to packaging within layer with solder balls 30 to make interconnections with integrated circuits 32 as shown on the Fig. 2 (col. 13, ll.25-28); b) a power grid comprising a plurality of metal layers for providing power to the at least one I/O circuit and the at least one logic circuit within plurality of power lines 45, 45a, 46, 46a, 48, 48a shown on the Fig. 2 for providing power for semiconductor device 32 on the power planes 23, 25 (col. 9, ll.20-25, ll.45-48); c) a semiconductor device layer in electrical communication with said power grid within semiconductor segments 32 shown on the Fig. 2, wherein semiconductor segments 32 include internal circuitry (col. 8, ll.15-16-18) and interconnected to the power planes 23 and 25 (col. 8, ll.23-25); and d) a wiring layer interposed between said contact layer and said power grid and electrically connecting said plurality of contacts with said power grid as shown on the Fig. 2, wherein wiring layer 19 is interposed between contact layer where contacts 30 are disposed and power grid 23 within power lines 45A (col. 8, ll.42-45), said wiring layer including a plurality of wires each having a length extending partly along a first direction and partly along a second direction different from said first direction within wiring layer 19, wherein wiring layer 19 has a plurality of wires (col. 8, , ll.47-50) as shown on the Fig. 2 (above via 14), wherein wires of the wiring layer 19 having width and length

extending in first direction and perpendicular to the first direction as an other direction as shown on the Fig. 2.

With respect to claim 18 Jacobs et al. teaches a device as shown on the Fig. 2, comprising: a) a power supply within power planes 11 shown on the Fig. (col. 11, ll.45-47); and b) an integrated circuit having at least one I/O circuit and at least one logic circuit, said integrated circuit comprising: i) a contact layer having a plurality of contacts in electrical communication with said power supply within layer with solder balls 30 to make interconnections with integrated circuits 32 as shown on the Fig. 2 (col. 13, ll.25-28); ii) a power grid comprising a plurality of metal layers for providing power to said at least one I/O circuit and said at least one logic circuit within plurality of power lines 45, 45a, 46, 46a, 48, 48a shown on the Fig. 2 for providing power for semiconductor device 32 on the power planes 23, 25 (col. 9, ll.20-25, ll.45-48); iii) a semiconductor device layer in electrical communication with said power grid within semiconductor segments 32 shown on the Fig. 2, wherein semiconductor segments 32 include internal circuitry (col. 8, ll.15-16-18) and interconnected to the power planes 23 and 25 (col. 8, ll.23-25); and iv) a wiring layer interposed between said contact layer and said power grid and electrically connecting at least some of said contacts with said power grid as shown on the Fig. 2, wherein wiring layer 19 is interposed between contact layer where contacts 30 are disposed and power grid 23 within power lines 45A (col. 8, ll.42-45), said wiring layer including a plurality of wires each having a length extending partly along a first direction and partly along a second direction different from said first direction within wiring layer 19, wherein wiring layer 19 has a plurality of wires (col. 8, , ll.47-50) as

shown on the Fig. 2 (above via 14), wherein wires of the wiring layer 19 having width and length extending in first direction and perpendicular to the first direction as an other direction as shown on the Fig. 2.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-4, 6-8, 11, 12, 14, 15, 17, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs et al. as applied to claims 1, 10 and 18 above, and further in view of Tsuyuki (US Patent 6,404,026).

With respect to claims 2-8, 11-15, 17, 19, 20 Jacobs et al. teaches the limitations from which the claims depend. However Jacobs et al. lacks the specifics regarding configuration of the wires. Tsuyuki teaches:

Claims 2 and 19: each of at least some of the plurality of wires have a ring-shaped configuration within the fixed potential wiring layers 18a and 18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50);

Claims 3 and 11: the ring-shaped configuration is rectangular within the fixed potential wiring layers 18a and 18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50);

Claims 5 and 13: the plurality of contacts includes a plurality of first contacts and a plurality of second contacts located alternatively with respect to the plurality of first contacts along a plurality of lines, the wiring layer including a plurality of first wires and a plurality of second wires wherein each of the plurality of second wires is laterally spaced from a corresponding one of the plurality of first wires, and each of the plurality of first wires is located on one side of a corresponding one of the plurality of lines and a corresponding one of the plurality of second wires is located on the opposite side of the corresponding one of the plurality of lines within the fixed potential wiring layers 18a and 18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50);

Claims 4, 12 and 20: at least some of the ones of the plurality of wires having the ring-shaped configuration are arranged concentrically with one another (col. 9, ll.50-57);
Claim 6: the plurality of wires is arranged in concentric rings within the semiconductor device having ability of the different configurations of the fixed potential wiring layer (ring) (col. 9, ll.50-57);

Claims 7 and 14: the plurality of wires includes a plurality of Vdd wires and a plurality of ground wires within the fixed potential wiring layers 18a and 18b shown on the Figs, 2, 3 and 5, wherein potentials may be set to a power and ground contacts (col. 4, ll.58-62; col. 6, ll.65-67);

Claims 8 and 15: a plurality of Vddx wires within the fixed potential wiring layers 18a and 18b shown on the Figs, 2, 3 and 5, wherein the fixed potential wiring layers 18a

and 18b are fixed at a potential of the semiconductor substrate 11 with desired values (col. 6, ll.60-65);

Claim 17: the power grid comprises a plurality of layers each comprising wires having longitudinal axes all extending in the same direction within the fixed potential wiring layers 18a and 18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50), wherein the extension of the wiring direction may be in any configuration (col. 9, ll.50-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Tsuyuki to teach the specifics Jacobs et al. does not teach, because of flexibility and various of effects and functions (col. 11, ll.52-54).

Allowable Subject Matter

8. Claims 9,16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art of record does not teach plurality of contacts is arranged in a square pattern having diagonal symmetry and major axis symmetry.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER